DASIP 2022: Workshop on Design and Architectures for Signal and Image Processing

in conjunction with the 17th HiPEAC Conference in Budapest, Hungary, January 17-19, 2022.

Chairs

Karol Desnos, IETR - FR

Sergio Pertuz, Technical University Dresden - DE

CALL FOR PAPERS

The **Workshop on Design and Architectures for Signal and Image Processing (DASIP)** provides an inspiring international forum for the latest innovations and developments in the field of leading signal, image and video processing and machine learning in custom embedded, edge and cloud computing architectures and systems. The workshop program will include keynote speeches and contributed paper sessions. The 15th edition will be held in conjunction with the 17th HiPEAC Conference in Budapest, Hungary, January 17-19, 2022.

SUBMISSION GUIDELINES

Authors should submit their full papers (up to 12 pages, single-column Springer format) in PDF through the EasyChair system. Please use the Spinger LNCS template.

Submitted papers are required to describe original unpublished work and must not be under consideration for publication elsewhere. Submissions must be fully anonymous, but authors should not hide previous work, instead, they need to make self-references in the third person. More details on submission requirements, templates and submission instructions are provided on the DASIP website.

Each submission will receive at least three independent double blind reviews from the members of our scientific committee. Authors will be encouraged to take the reviewers' comments into account when they prepare the final versions of their papers and present the research during the workshop prior to its publication. The conference proceedings will be published in the Springer LNCS Series, on the Springer Link website. Paper and keynote presentation slides and tutorial documents will be made available to workshop attendees after the workshop (subject to confidentiality issues). Authors of the best papers will be invited to submit an extended version of their work to Elsevier's Journal of System Architecture.

IMPORTANT DATES (ALL 23:59 A.O.E)

- Abstract submission deadline: November 5th, 2021
- Paper submission deadline: **November 12th, 2021**
- Notification of acceptance: December 20th, 2021
- Camera ready papers: January 7th, 2022
- Workshop : January 17-19, 2022

VENUE

The Workshop on Design and Architectures for Signal and Image Processing will be held in conjunction with the 17th HiPEAC Conference in Budapest, Hungary, January 17-19, 2022.

CONTACT

All questions about the workshop and submissions should be emailed to Karol Desnos <karol.desnos@insa-rennes.fr>, Marcelo Brandalero <marcelo.brandalero@b-tu.de>, or Sergio Pertuz <sergio.pertuz@tu-dresden.de>.

LIST OF TOPICS

Prospective authors are invited to submit manuscripts on topics including, but not limited to:

Custom embedded, edge and cloud architectures and systems:

- Machine learning and deep learning architectures for inference and training
- Systems for autonomous vehicles : cars, drones, ships and space applications
- Image processing and compression architectures
- Smart cameras, security systems, behaviour recognition
- Edge and cloud processing: special routing, configurable co-processors and low energy considerations
- Real-time cryptography, secure computing, financial and personal data processing
- Computer arithmetic, approximate computing, probabilistic computing, nanocomputing, bio-inspired computing
- Biological data collection and analysis, bioinformatics
- Personal digital assistants, natural language processing, wearable computing and implantable devices
- Global navigation satellite and inertial navigation systems

Design Methods and Tools:

- Design verification and fault tolerance
- Embedded system security and security validation
- System-level design and hardware/software co-design
- High-level synthesis, logic synthesis, communication synthesis
- Embedded real-time systems and real-time operating systems
- Rapid system prototyping, performance analysis and estimation
- Formal models, transformations, algorithm transformations and metrics

Development Platforms, Architectures and Technologies:

- Embedded platforms for multimedia and telecommunication
- Many-core and multi-processor systems, SoCs, and NoCs
- Reconfigurable ASIPs, FPGAs, and dynamically reconfigurable systems
- Memory system and cache management
- Asynchronous (self-timed) circuits and analog and mixed-signal circuits

STEERING COMMITTEE