DASIP 2021: Workshop on Design and Architectures for Signal and Image Processing

in conjunction with the 16th HiPEAC Conference in Budapest, Hungary, January 18-20, 2021.

Virtual event

Chairs:

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Andrea Pinna, Sorbonne Universite, Paris, France

2ND CALL FOR PAPERS

The **Workshop on Design and Architectures for Signal and Image Processing (DASIP)** provides an inspiring international forum for the latest innovations and developments in the field of leading signal, image and video processing and machine learning in custom embedded, edge and cloud computing architectures and systems. The workshop program will include keynote speeches and contributed paper sessions. The 14th edition will be held in conjunction with the 16th HiPEAC Conference in Budapest, Hungary, January 18-20, 2021. Due to the current Covid-19 situation the HiPEC'21 conference will be a virtual event.

SUBMISSION GUIDELINES

Authors should submit their full papers (up to 12 pages, single-column ACM format) in PDF through the EasyChair system. Please use the ACM template (Latex only, Master Article Template - sample-manuscript.tex). It is also available in Overleaf (ACM Conference Proceedings "Master" Template).

Submitted papers are required to describe original unpublished work and must not be under consideration for publication elsewhere. Submissions must be fully anonymous, but authors should not hide previous work, instead, they need to make self-references in the third person. More details on submission requirements, templates and submission instructions are provided on the DASIP website.

Each submission will receive at least three independent double blind reviews from the members of our scientific committee. Authors will be encouraged to take the reviewers' comments into account when they prepare the final versions of their papers and present the research during the workshop prior to its publication. The workshop proceedings will be published in the ACM International Conference Proceedings Series (ICPS). Paper and keynote presentation slides and tutorial documents will be made available to workshop attendees after the workshop (subject to confidentiality issues).

The authors of DASIP 2021 **best papers** will be invited to submit an extended version of their work to a **special issue** in Journal of Signal Processing Systems (JSPS).

IMPORTANT DATES (ALL 23:59 A.O.E)

- Abstract submission deadline: ~~October 11th, 2020,~~ October 25th, 2020
- Paper submission deadline: ~~**October 18th, 2020**~~, **November 01st, 2020**
- Notification of acceptance: ~~November 22th, 2020~~, November 30th, 2020
- Camera ready papers: December 6th, 2020
- Workshop : January 18-20, 2021

VENUE

The Workshop on Design and Architectures for Signal and Image Processing will be held in conjunction with the 16th HiPEAC Conference in Budapest, Hungary, January 18-20, 2021. Due to the current Covid-19 situation, it will be a **virtual event**.

WORKSHOP FORMAT

We would like to propose a workshop format to have the research results presented with an in-depth scientific discussion without unnecessary time pressure:
- presentation time 20 min + 10 min for questions and discussion,
- additional 1-2 sessions devoted to discussion on topics selected by the participants,
- interesting keynotes.

CONTACT

All questions about the workshop and submissions should be emailed to :
- Tomasz Kryjak <tomasz.kryjak@agh.edu.pl> or
- Andrea Pinna <andrea.pinna@sorbonne-universite.fr>.

LIST OF TOPICS

Prospective authors are invited to submit manuscripts on topics including, but not limited to:

Custom embedded, edge and cloud architectures and systems:
- Machine learning and deep learning architectures for inference and training
- Systems for autonomous vehicles : cars, drones, ships and space applications
- Image processing and compression architectures
- Smart cameras, security systems, behaviour recognition
- Edge and cloud processing: special routing, configurable co-processors and low energy considerations
- Real-time cryptography, secure computing, financial and personal data processing
- Computer arithmetic, approximate computing, probabilistic computing, nanocomputing, bio-inspired computing
- Biological data collection and analysis, bioinformatics
- Personal digital assistants, natural language processing, wearable computing and implantable devices
- Global navigation satellite and inertial navigation systems

Design Methods and Tools:
- Design verification and fault tolerance
- Embedded system security and security validation
- System-level design and hardware/software co-design
- High-level synthesis, logic synthesis, communication synthesis
- Embedded real-time systems and real-time operating systems
- Rapid system prototyping, performance analysis and estimation
- Formal models, transformations, algorithm transformations and metrics

Development Platforms, Architectures and Technologies:
- Embedded platforms for multimedia and telecommunication
- Many-core and multi-processor systems, SoCs, and NoCs
- Reconfigurable ASIPs, FPGAs, and dynamically reconfigurable systems
- Memory system and cache management
- Asynchronous (self-timed) circuits and analog and mixed-signal circuits

STEERING COMMITTEE

- Bertrand Granado, Sorbonne Université
- Diana Goehringer, TU Dresden
- Eduardo de La Torre, Universidad Politecnica de Madrid
- Guy Gogniat, Université de Bretagne Sud - UEB
- Jean-Francois Nezan, INSA Rennes/ IETR laboratory
- Jean-Pierre David, Ecole Polytechnique de Montreal
- Joao M. P. Cardoso, University of Porto
- Marek Gorgon, AGH University of Science and Technology
- Michael Huebner, Brandenburg University of Technology
- Paolo Meloni, University of Cagliari
- Pierre Langlois, Ecole Polytechnique de Montreal
- Sebastien Pillement, University of Nantes - IETR
- Tomasz Kryjak, AGH University of Science and Technology